#21
5-25-03
NP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Date: May 15, 2003
Express Mail: ER216392565US

In re application of: **J. S. Beeteson, et al**

Serial No.: **09/170,336**

Filed: **October 13, 1998**

Docket No.: **UK998-026**

Board of Patent Appeals and Interferences
Washington, D.C. 20231

TRANSMITTAL OF APPEAL BRIEF UNDER 37 CFR 1.192

Sir:

Transmitted herewith, in triplicate is an Appeal Brief with respect to the Notice of Appeal filed March 17, 2003 for the above-identified patent application.

This Appeal Brief is being filed on behalf of other than a small entity.

Authorization is given to charge amount of $320.00, for filing a Brief in support of appeal in accordance with 37 CFR 1.17(f), to Deposit Account 50-0510. A duplicate copy of this authorization is enclosed.

The Assistant Commissioner is hereby authorized to charge any required additional fee, and charge back any overpayment, to Deposit Account No. 50-0510.

Respectfully submitted,
J. S. Beeteson, et al

Anne Vachon Dougherty
Registration No. 30,374
Tel. (914) 962-5910

#21
5-25-03
NP

Serial No. 09/170,336
Art Unit No. 2674

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS
BEING DEPOSITED IN EXPRESS MAIL AS
EXPRESS MAIL: ER216392565US ON
DATE OF DEPOSIT: May 15, 2003
PERSON DEPOSITING: ANNE VACHON DOUGHERTY

Anne Vachon Dougherty 5/15/03
Signature & Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of :	May 15, 2003
J. S. Beeteson, et al :	Group Art No.: 2674
Serial No. 09/170,336 :	Examiner: K. M. Nguyen
Filed: October 13, 1998 :	IBM Corporation by Anne Vachon Dougherty 3173 Cedar Road Yorktown Hts, NY 10598
Title: ACTIVE CORRECTION TECHNIQUE FOR A MAGNETIC MATRIX DISPLAY	

Board of Patent Appeals and Interferences
Washington, D.C. 20231

APPEAL BRIEF (37 CFR 1.192)

Applicant hereby appeals to the Board of Patent Appeals and Interferences from the decision dated October 15, 2002 of the Primary Examiner finally rejecting Claims 1-11 in the above application, and respectfully request that the Board

of Patent Appeals and Interferences consider the arguments presented herein and reverse the Examiner's rejection.

I. REAL PARTY IN INTEREST

The appeal is made on behalf of Applicants who are real parties in interest with respect to the subject patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no pending related appeals or interferences with respect to the subject patent application.

III. STATUS OF CLAIMS

There are eleven (11) claims pending in the subject patent application, numbered 1-11. No claims stand allowed. All of Claims 1-11 stand rejected.

A complete copy of the claims involved in the appeal is attached hereto.

IV. STATUS OF AMENDMENTS

The status of the prosecution of the application is as follows:

May 9, 2000	-	Office Action.
September 8, 2000	-	Amendment
November 2, 2000	-	Office Action
January 30, 2001	-	Amendment
March 7, 2001	-	Office Action
July 9, 2001	-	Amendment
September 25, 2001	-	Final Office Action
February 25, 2002	-	CPA and Amendment
April 24, 2002	-	Office Action
July 24, 2002	-	Amendment
October 15, 2002	-	Final Office Action
March 17, 2003	-	Notice of Appeal

V. SUMMARY OF INVENTION

The subject invention is a matrix-addressed display device having a cathode means; a grid electrode means, wherein the grid electrode means comprises a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors; and, a means for providing cut-off correction information and gain correction information to one of the first plurality or the second plurality of conductors.

VI. STATEMENT OF ISSUES OF APPEAL

There following issues are on appeal:

(1) whether the Examiner correctly stated the claimed invention when rejecting the sole independent claim, Claim 1;

(2) whether the display device as recited in Claim 1 is patentable over the combined teachings of

the Applicants' Admitted Prior Art (hereinafter "AAPA") and the Nakamura patent (USP 5,818,403);

(3) whether the display device as claimed in Claim 2 is patentable over the combined teachings of the AAPA, the Nakamura patent, and the Buzak patent (USP 5,036,317);

(4) whether the display device as claimed in Claims 3-7 is patentable over the combined teachings of the AAPA, the Nakamura patent, the Buzak patent, and the Baldi patent (USP 5,708,451); and

(5) whether the display device as claimed in Claim 8-11 is patentable over the combined teachings of the AAPA, the Nakamura patent, the Buzak patent, the Baldi patent, and the Tanaka patent (USP 5,834,900).

VII. GROUPING OF CLAIMS

The Claims can be considered in the following groups for purposes of this appeal:

(I) Group I: Claims 1-2, wherein the matrix addressed display device is detailed to include the cathode means, grid electrode means comprising a first plurality of row conductors and a second plurality of column conductors, and means for providing cut-off correction information (Claim 1) and gain correction information (Claim 2) to one of the first plurality or the second plurality of conductors;

(II) Group II: Claims 3-4, the device of Claim 1 further comprising memory (Claim 3) and screen (Claim 4);

(III) Group III; Claims 5-7, the device as recited in Claim 1 and further comprising applying correction information to only the first plurality of conductors (Claim 5) and wherein correction information is chosen to compensate for variations during warm up (Claims 6-7);

(IV) Group IV; Claims 8-11, the device as recited in Claim 1 wherein temperature and location affect the values of the cut-off and gain correction information to be supplied.

VIII. ARGUMENT

ARGUMENT (1)

With regard to issue (1), whether the Examiner correctly stated, and correctly examined, the claimed invention when rejecting the sole independent claim, Claim 1, Applicants refer the Board's attention to the language of Claim 1 and to the Examiner's statement on page 3 of the Final Office Action from which Applicants are appealing. The language of Claim 1 recites "[a] matrix addressed display device comprising: a cathode means; grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors; characterised in that the display device further comprises: means for providing cut-off correction information to ***one of said first or said second plurality of parallel conductors***" (emphasis added). In contrast, the Examiner has stated, on page 3, paragraph 6, lines 7-8, "means for providing cut-off correction information to a ***one of said first of*** parallel conductors".

Applicants respectfully assert that the Examiner has restated the claim language in order to make the cited references applicable. Applicants are not claiming a means for providing cut-off correction information to one of a first of parallel conductors. Applicants are claiming a means for providing cut-off correction information to one of said first or said second plurality of parallel conductors. Applicants respectfully argue that the Examiner has not correctly stated the claim language and has not, as a result, correctly examined the invention as claimed.

ARGUMENT (2)

As to issue (2), whether the display device as recited in Claim 1 is patentable over the combined teachings of the Applicants' Admitted Prior Art (hereinafter "AAPA") and the Nakamura patent (USP 5,818,403); Applicants submit the following arguments.

The subject application teaches and claims a matrix addressed display device comprising a cathode means, grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors; and

allows the cut-off of individual rows or columns to be adjusted, so as to reduce luminance variations." The Specification goes on to teach that all of the plurality of conductors can receive the same correction information, as in the "warm up" correction situation taught at page 11, lines 16-18, or each of the plurality of conductors can receive a specific correction value based on its position in the array, as taught in the luminance variation situation taught at page 17, lines 20-25. In either case, ***all*** of the conductors in a plurality of conductors are receiving correction information along with the drive voltage information. Accordingly, what is taught and claimed is an device whereby the image information (e.g., cut-off voltage or a voltage below cut-off), and correction information is being supplied to all of a plurality of conductors.

The Applicants' Admitted Prior Art, AAPA, from the Specification at page 1, lines 16-21 is a magnetic matrix display. The Examiner states, on page 3, paragraph 6 of the Office Action, that "AAPA teaches a magnetic matrix display which includes a cathode 20...AAPA fails to teach a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the

means for providing cut-off correction information to a one of said first or said second plurality of parallel conductors, as is specifically recited in independent Claim 1, and all of the remaining claims which depend therefrom.

Under the present invention, cut-off correction information and, optionally, gain correction information as well, is provided to one of a first plurality of parallel conductors (e.g., rows) or a second plurality of parallel conductors (e.g., columns) along with the drive voltage information which is being provided to those conductors based on the image display desired. As set forth in the teachings found from lines 11-27 on page 12 of the Specification, "[w]hen a particular column driver is not selected, the column grid conductor...is driven to a non-selected voltage, that is a voltage below cut-off" and "when a column driver 502 is selected...[it is] driven to a cut-off voltage" and "[t]he level of drive to the...conductors is determined by the pixel data...and the correction data 516 supplied from...memory. The correction data 516 consists of cut-off and gain corrections."

As further taught in the Specification at page 6, lines 19-23, "[t]he provision of cut-off correction information

row conductors, means for providing cut-off correction information to a one of said first of parallel conductors." The Examiner then goes on to cite the Nakamura patent as providing those teachings that are missing from the AAPA. Applicants acknowledge that the AAPA teaches a magnetic matrix display with a cathode and that the AAPA magnetic matrix display does not include the additionally recited claim features.

The Nakamura patent teaches a driving method for an electron beam generation system with image forming apparatus associated therewith. The Nakamura system includes rows of parallel electron-emitting device lines arranged in an XY matrix with columns of parallel modulation electrodes. The Nakamura method comprises alternately applying information signals to odd-numbered rows of electrodes in a parallel array of rows while applying cut-off information signals to the even-numbered electrodes in the parallel array; and, then, reversing the process to apply information signals to even-numbered rows of electrodes while applying cut-off information signals to the odd-numbered electrodes (see: e.g., Col. 5, line 65 through Col. 6, line 5). Nakamura alternates application of its signals in order to reduce the

negative (e.g., capacitance) effects experienced between neighboring modulation electrodes (see: e.g., Col. 5, line 46-50).

It is first to be noted that the Nakamura meaning of the term "cut-off" is actually not consistent with the meaning of "cut-off" in the present application. The Nakamura patent uses the term "cut-off" to mean non-information signals to be applied to non-selected rows (e.g., the even rows) to suppress conduction therein; while the present invention uses the term "cut-off" to mean the voltage applied to all selected conductors, in accordance with the formula detailed on pages 5-6 of the Specification for reducing luminance variations (see: page 6, lines 20-23). Further, what Nakamura teaches is the application of cut-off voltage alone and not the provision of additional signal correction information to the conductors. Finally, it is quite clear in Nakamura that the cut-off signals are being applied to only half of the electrodes in a plurality of electrodes (the driving method detailed at Col. 5, lines 41-46), whereas the present invention is teaching and claiming the application of correction information to all of

the first plurality of row conductors or to all of the second plurality of column conductors.

Since the Nakamura method is directed to alternately applying signals to the odd and even numbered columns in one plurality of conductors, Applicants respectfully argue that one having skill in the art would not be motivated by the Nakamura teachings to apply a signal to all of a plurality of row conductors or all of a plurality of column conductors. Applicants believe that Nakamura clearly teaches away from such an embodiment.

Applicants further note that to suggest that the current be applied to all rows or columns would render the Nakamura teachings unworkable, since applying the signals to all neighboring rows would be inconsistent with the Nakamura teaching of alternate application of voltage to reduce negative effects. Clearly the Nakamura reference does not include any suggestion of such application of information to all rows or all columns. Moreover, since to modify the Nakamura teachings to apply the information to all rows or all columns would make it unworkable for its intended purpose, such could not be considered obvious. It is well established under U.S. Patent Law that modification of

teachings cannot be considered obvious to one having skill in the relevant art if such modification would render the teachings unworkable for their intended purpose. Clearly, therefore, it cannot be maintained that the teachings of the Nakamura reference obviate the invention as claimed.

Applicants believe that a combination of the teachings of the AAPA and the teachings of the Nakamura patent would not render the present invention obvious. If one were motivated to combine the teachings, one would arrive at a magnetic matrix display driven by a Nakamura driving method of applying cut-off voltage to alternate rows of electrodes while applying information signals to the other parallel rows. Clearly such a combination would not obviate the invention as claimed comprising a cathode means, grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors, and means for providing cut-off correction information to a one of said first or said second plurality of parallel conductors (Claim 1).

ARGUMENT (3)

As to issue (3), whether the display device as claimed in Claim 2 is patentable over the combined teachings of the AAPA, the Nakamura patent, and the Buzak patent (USP 5,036,317), Applicants submit the following arguments. The Examiner has rejected Claim 2 as unpatentable over the AAPA in view of Nakamura as applied to claim 1 and further in view of Buzak. Applicants rely on the arguments presented above in "ARGUMENT (2)" with regard to the applicability of the AAPA in combination with the Nakamura patent.

Claim 2 additionally recited "means for providing gain correction information to a one of said first or said second plurality of parallel conductors." In citing the Buzak patent, the Examiner states that the Buzak patent "teaches display system 40 having nine different output amplifiers 86, data driver 88 driving the amplifiers for different ones of column electrodes 62".

The Buzak patent is directed to a flat panel display having columns electrodes on a first substrate which receive data drive signals and rows on a second substrate addressed by electron beams. The cited teachings of Buzak at Col. 12, lines 34-39 teach that the system may have multiple output

amplifiers with the one data driver. Applicants respectfully contend that having a single data driver with multiple output amplifiers does not obviate the claimed means for providing gain correction, since Buzak provides no teachings of providing gain correction via its data driver 88. Moreover, the Buzak patent does not teach or suggest that a signal (be it gain correction or another signal) be applied to all of a plurality of parallel conductors. Applicants respectfully conclude that the combination of AAPA, Nakamura, and Buzak does not obviate the invention claimed by Claim 2.

ARGUMENT (4)

As to issue (4), whether the display device as claimed in Claims 3-7 is patentable over the combined teachings of the AAPA, the Nakamura patent, the Buzak patent, and the Baldi patent (USP 5,708,451), Applicants submit the following arguments. The Examiner has rejected Claims 3-7 as unpatentable over the AAPA in view of Nakamura and Buzak as applied to claims 1 and 2, and further in view of Baldi. Applicants rely on the arguments presented above in "ARGUMENT (2)" and "ARGUMENT (3)" with regard to the

applicability of the AAPA in combination with Nakamura and Buzak. In rejecting Claims 3-7, the Examiner has cited the Baldi patent. Applicants respectfully argue that any such combination would not render the Claims 3-7 obvious.

The Baldi patent teaches several circuit arrangements for supplying a single signal to column conductors in a matrix. Each of the circuit arrangements provided by the Baldi patent has one or more correction circuits which take both the drive voltage and a correction signal and output a single signal to one or more columns. If one were to combine the teachings of the Baldi patent with that of the AAPA, Nakamura and Buzak, the resulting system would include (a) at least one correction circuit for receiving a drive signal plus a correction signal and for outputting a single combined signal (i.e., the information signal of Nakamura) to a first set of columns (e.g., the even columns) and (b) the cut-off signal circuitry of Nakamura for providing a cut-off signal to the alternate set of columns (e.g., the odd columns). Clearly, therefore, even if one were motivated to combine the references, one would not arrive at the invention as set forth in the pending claims.

With regard to Claim 3, while Baldi has a non-volatile memory, such is not sufficient, in combination with the other cited teachings, to render Claim 3 obvious, since the combination would not include a matrix addressed display device comprising a cathode means; grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors; characterised in that the display device further comprises: means for providing cut-off correction information to one of said first or said second plurality of parallel conductors, further comprising means for providing gain correction information to one of said first or said second plurality of parallel conductors and further comprising a non-volatile memory for storing a plurality of values for said cut-off and gain correction information.

With regard to Claim 4, while the AAPA teaches that the surface of the magnet faces the phosphors, such does not, in combination with the other cited references, obviate the Claim 4 language of a matrix addressed display device comprising: a cathode means; grid electrode means comprising a first plurality of parallel row conductors and a second

plurality of parallel column conductors arranged orthogonally to the row conductors; characterised in that the display device further comprises: means for providing cut-off correction information to one of said first or said second plurality of parallel conductors, means for providing gain correction information to one of said first or said second plurality of parallel conductors, a non-volatile memory for storing a plurality of values for said cut-off and gain correction information, and further comprising a screen for receiving electron beams modulated by said grid electrode means, the screen having a phosphor coating facing the grid electrode means, the phosphor coating comprising a plurality of pixels each corresponding to a different row or column.

With regard to Claim 5, while Buzak teaches amplifiers for different single column electrodes, such is clearly not the same as or suggestive of means for providing gain and cut-off correction information to all of a first plurality of parallel conductors. In fact, having such dedicated amplifiers teaches away from the invention as recited in Claim 5 wherein cut-off and gain correction information is applied to all of the first plurality of parallel

conductors. Applicants further argue that the Buzak teachings of dedicated amplifiers, and of forming an electro beam does not, in combination with the other cited references, obviate the Claim 5 language of a matrix addressed display device comprising: a cathode means; grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors; characterised in that the display device further comprises: means for providing cut-off correction information to one of said first or said second plurality of parallel conductors, means for providing gain correction information to one of said first or said second plurality of parallel conductors, a non-volatile memory for storing a plurality of values for said cut-off and gain correction information, wherein said cut-off and gain correction information is provided to said first plurality of parallel conductors, said gain and cut-off correction information being applied to all of said first plurality of parallel conductors.

As to Claim 6, the Baldi mention in the abstract of pixel correction factors for compensating long-term decline of luminance due to phosphor aging does not teach or suggest

that values for cut-off and gain correction are chosen to compensate for variations in cut-off and gain which occur during warm up, let alone that feature in combination with the other claim features of a matrix addressed display device comprising: a cathode means; grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors; characterised in that the display device further comprises: means for providing cut-off correction information to one of said first or said second plurality of parallel conductors, means for providing gain correction information to one of said first or said second plurality of parallel conductors, a non-volatile memory for storing a plurality of values for said cut-off and gain correction information. Baldi provide no teaching or suggestion that aging degradation is analogous to warm up variations. Moreover, the Baldi proposed solution for addressing nonuniformity is to generate correction values for each pixel (see: e.g., Col. 5, lines 55-62) which must, necessarily be selectively applied (Col. 7, lines 6-11) in order to deal with the nonuniformity. Clearly, the Baldi selective application for addressing pixel variations is not

the same as or suggestive of applying gain or cut-off correction signals to all of a plurality of conductors.

With regard to Claim 7, which additionally recites the anode means and means for providing purity correction information, Applicants respectfully assert that the AAPA does detail anode means disposed between said grid electrode means and said screen for accelerating electrons towards the screen, but does not detail the anode means comprising a plurality of anodes extending parallel to the column conductors, the anode means comprising pairs of anodes each corresponding to a different column conductor, each pair comprising first and second anodes respectively extending along opposite sides of the corresponding column conductor, the first anodes being interconnected and the second anodes being interconnected (see, page 1) and means for providing purity correction information as claimed.

Further the Baldi patent mention of pixel correction factors to compensate for long term decline is not the same as nor suggestive of the claimed means for providing purity correction information across the first and second anodes so as to compensate for variations in purity occurring during warm up. Applicants respectfully assert that the Examiner

is again restating the claim language, here to "compensating long term decline of luminance due to the phosphors ageing (*sic*) process" (page 5) to allow the cited art to apply. Baldi does not teach or suggest the application of cut-off or gain correction information to all of a plurality of parallel conductors in conjunction with the application of purity correction information across first and second anodes to compensate for variations in purity. Applicants respectfully assert that the combination does not obviate the invention as is recited in the claim, including a matrix addressed display device comprising: a cathode means; grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors; characterised in that the display device further comprises: means for providing cut-off correction information to one of said first or said second plurality of parallel conductors, means for providing gain correction information to one of said first or said second plurality of parallel conductors, a non-volatile memory for storing a plurality of values for said cut-off and gain correction information, wherein the cut-off and gain correction information is chosen so as to

compensate for variations in cut-off and gain occurring during warm up and further comprising anode means disposed between said grid electrode means and said screen for accelerating electrons towards the screen, the anode means comprising a plurality of anodes extending parallel to the column conductors, the anode means comprising pairs of anodes each corresponding to a different column conductor, each pair comprising first and second anodes respectively extending along opposite sides of the corresponding column conductor, the first anodes being interconnected and the second anodes being interconnected; and means for providing purity correction information across the first and second anodes so as to compensate for variations in purity occurring during warm up.

ARGUMENT (5)

As to issue (5), whether the display device as claimed in Claim 8-11 is patentable over the combined teachings of the AAPA, the Nakamura patent, the Buzak patent, the Baldi patent, and the Tanaka patent (USP 5,834,900), Applicants submit the following arguments. Claims 8-11 all include the limitations of Claims 1-3. Accordingly, Applicants rely on

the arguments set forth above in "ARGUMENT (2)" and "ARGUMENT (3)" and will not reiterate the same arguments. Further, Claim 8 depends from Claim 6 and Applicants rely on the arguments set forth in "ARGUMENT (5)" in support of Claim 8. In rejecting Claims 8-11, the Examiner has additionally cited the Tanaka patent.

The Tanaka patent is cited against Claim 8 for teachings an FED device having a temperature sensor. The Tanaka patent is directed to a system having X and Y drivers for maintaining a constant differential voltage between its gate voltage and its cathode voltage regardless of the drive voltage (see: Col. 3, lines 60-63). Based on temperature sensing at the temperature sensor (Col. 6, line 31), when an increase in temperature is detected, as the electrodes are selectively driven row by row in order (see: Col. 4, lines 66-67), the differential voltage will change. Accordingly, a variation of the gate voltage, which variation is linear with respect to the temperature, is applied to compensate for the temperature increase.

Applicants respectfully assert that the Tanaka teachings do not, alone or in combination with the other cited references, render the present invention obvious.

First of all, Tanaka varies the gate voltage and does not apply a cut-off or gain correction voltage per se. Further, Tanaka expressly teaches that the gate voltage is applied row by row in order. Clearly modifying Nakamura, etc. with Tanaka would not result in the present invention wherein cut-off or gain correction is applied to all of the parallel rows or columns. Rather, the combination would result in either row-by-row or alternating application of gate voltage, but not the invention as claimed.

With regard to Claims 9-11, all of which recite the cut-off and/or correction voltages varying according to physical location, Applicants again assert that the Tanaka patent teachings would not obviate the claims, alone or in combination with the other cited references. The Examiner states that Tanaka teaches "a (sic) FED which includes the cathode electrodes with respect to a cut-off voltage are deviated from a set point, the cathode current is varied with respect the (sic) column voltage." What Tanaka teaches is that the gate or cathode voltage is varied to maintain the constant differential voltage in response to variations in temperature. The voltage is not varied based on location and is not different for different gate lines or cathode

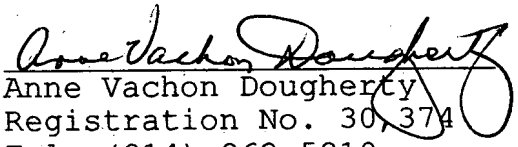
lines due to their location. Clearly the Examiner has erred in applying the Tanaka teachings to the language of Claims 9-11.

CONCLUSION

Applicants respectfully assert that the Examiner has erred in stating Claim 1, and in rejecting Claim 1 as unpatentable over the combination of AAPA with Nakamura, Claim 2 as unpatentable over AAPA with Nakamura in view of Buzak, Claims 3-7 as unpatentable over AAPA with Nakamura in view of Buzak and Baldi, and Claims 8-11 as unpatentable over AAPA with Nakamura in view of Buzak, Baldi and Tanaka. Applicants believe that the Examiner has selectively reworded the claim language to fit the teachings of the references, that the references do not provide the teachings which the Examiner has suggested, and that the combinations of teachings do not obviate the claims.

In light of the foregoing arguments, Applicants request that the decision of the Examiner, rejecting all of the pending claims, be overturned by the Board and that the claims be passed to issuance.

Respectfully submitted,
J. S. Beeteson, et al

By: 
Anne Vachon Dougherty
Registration No. 30,374
Tel. (914) 962-5910

APPENDIX OF CLAIMS

1. A matrix addressed display device comprising:

a cathode means;

grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors;

characterised in that the display device further comprises:

means for providing cut-off correction information to one of said first or said second plurality of parallel conductors.

2. A display device as claimed in claim 1 further comprising means for providing gain correction information to one of said first or said second plurality of parallel conductors.

3. A display device as claimed in claim 2 further comprising a non-volatile memory for storing a plurality of values for said cut-off and gain correction information.

4. A display device as claimed in claim 3, further comprising a screen for receiving electron beams modulated by said grid electrode means, the screen having a phosphor coating facing the grid electrode means, the phosphor coating comprising a plurality of pixels each corresponding to a different row or column.

5. A display device as claimed in claim 3, wherein said cut-off and gain correction information is provided to said first plurality of parallel conductors, said gain and cut-off correction information being applied to all of said first plurality of parallel conductors.

6. A display device as claimed in claim 3, wherein said cut-off and gain correction information is chosen so as to compensate for variations in cut-off and gain occurring during warm up.

7. A display device as claimed in claim 6, further comprising:

anode means disposed between said grid electrode means and said screen for accelerating electrons towards the screen, the anode means comprising a plurality of anodes extending parallel to the column conductors, the anode means comprising pairs of anodes each corresponding to a different column conductor, each pair comprising first and second anodes respectively extending along opposite sides of the corresponding column conductor, the first anodes being interconnected and the second anodes being interconnected; and

means for providing purity correction information across the first and second anodes so as to compensate for variations in purity occurring during warm up.

8. A display device as claimed in claim 6, further comprising temperature sensing means for determining which of said plurality of values of stored cut-off and gain correction information is supplied to a one of said first or said second plurality of parallel conductors.

9. A display device as claimed in claim 3, wherein said cut-off correction information is provided to said second plurality of parallel conductors, said cut-off correction information varying according to the physical location of each of said second plurality of parallel conductors.

10. A display device as claimed in claim 3, wherein said gain correction information is provided to said second plurality of parallel conductors, said gain correction information varying according to the physical location of each of said second plurality of parallel conductors.

11. A display device as claimed in claim 3, wherein said cut-off and gain correction information is provided to said first plurality of parallel conductors, said cut-off and gain correction information varying according to the physical location of each of said first plurality of parallel conductors and according to which of said second plurality of parallel conductors is selected.